Am25S05

Four-Bit by Two-Bit Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.

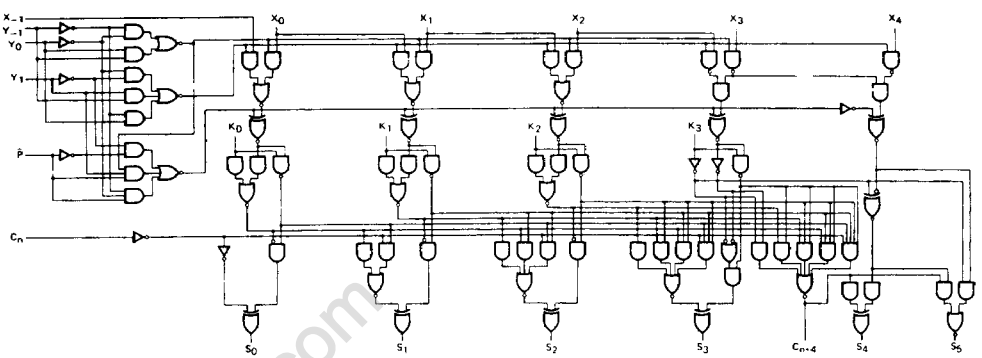
GENERAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m + n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

BLOCK DIAGRAM



BD001580

RELATED PRODUCTS

Part No.	Description
Am25LS14A	8-Bit Serial/Parallel Multiplier
Am25LS557/8	8-Bit by 8-Bit Multiplier
Am29516/7	16-Bit by 16-Bit Multiplier

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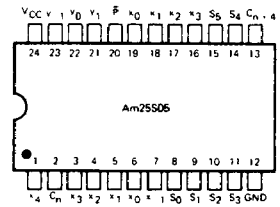
CONNECTION DIAGRAM
Top View



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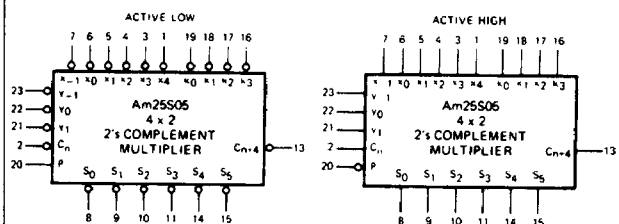
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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METALLIZATION AND PAD LAYOUT

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25S05 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 24-pin CERDIP
  - F– 24-pin flatpak
  - P– 24-pin plastic DIP
  - X– Dice
- **Am25S05** — Device type
  - 4-Bit by 2-Bit Multiplier

Valid Combinations	
Am25S05	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.
I Input.
L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.
O Output.

FUNCTIONAL TERMS:

C_n The carry input to the high-speed adder.
C_{n+4} The carry output from the high-speed adder.
K_i The constant field used for accumulating partial products. i = 0, 1, 2, 3. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.
$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.
S_i The product outputs. i = 0, 1, 2, 3, 4, 5.
x_i The multiplicand inputs. i = −1, 0, 1, 2, 3, 4. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.
Y_i The multiplier inputs. i = −1, 0, 1.
At the first row of the array Y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.
I_{OH} Output HIGH current, forced out of output in V_{OH} test.
I_{OL} Output LOW current, forced into the output in V_{OL} test.
I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.
I_{IH} Reverse input load current.
Negative Current Current flowing out of the device.
Positive Current Current flowing into the device.
V_{IH} Minimum logic HIGH input voltage.
V_{IL} Maximum logic LOW input voltage.
V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.
V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.
V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load	
	HIGH	LOW
Advanced Micro Devices 54/7400 Series	1.25	1.25
Advanced Micro Devices 9300/2500 Series	1.25	1.25
FSC Series 9300	1.25	1.25
TI Series 54/7400	1.25	1.25
Signetics Series 8200	2.5	2.5
National Series DM 75/85	1.25	1.25
DTL Series 930	15	1.25

OPERATION TABLE

Y Multiplier			Operation X Multiplicand
Y_{-1}	Y_0	Y_1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K − 2X
1	0	1	K − X
0	1	1	K − X
1	1	1	K − 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

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Am25S05 LOADING RULES IN UNIT LOADS

Input/Output	Pin Nos.	Input Unit Load: Input HIGH	Input Unit Load: Input LOW	Fan-out: Output HIGH	Fan-out: Output LOW
x_4	1	0.2	0.2	–	–
C_n	2	0.2	0.2	–	–
x_3	3	0.2	0.2	–	–
x_2	4	0.4	0.4	–	–
x_1	5	0.4	0.4	–	–
x_0	6	0.4	0.4	–	–
x_{-1}	7	0.2	0.2	–	–
S_0	8	–	–	20	10
S_1	9	–	–	20	10
S_2	10	–	–	20	10
S_3	11	–	–	20	10
GND	12	–	–	–	–
C_{n+4}	13	–	–	20	10
S_4	14	–	–	20	10
S_5	15	–	–	20	10
k_3	16	2	2	–	–
k_2	17	2	2	–	–
k_1	18	2	2	–	–
k_0	19	2	2	–	–
$\overline{P}$	20	1	1	–	–
y_1	21	0.6	0.6	–	–
y_0	22	0.6	0.6	–	–
y_{-1}	23	0.6	0.6	–	–
V_{CC}	24	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and −2.0mA at 0.5V at the LOW Logic Level.

USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the Y_i multiplier bit to the appropriate carry input terminal i = 1, 3, 5...
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number Representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s Y_s$ at K inputs
Unsigned (Magnitude)	Extended multiplier and multiplicand one bit at the least significant end. Form $x_0y_0 + y_0x + x_0y$ with conditional adder and add to array shifted two places up at k inputs. Force k_s, y_s, $x_s = 0$.
Sign magnitude	$x_s = 0$, $y_s = 0$ None $x_s = 1$, $y_s = 0$ Form $[(XY)_2 + 2^{n-1}y]$ $x_s = 0$, $y_s = 1$ Form $[(XY)_2 + 2^{n-1}x]$ $x_s = 1$, $y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

CONNECTION SCHEMES

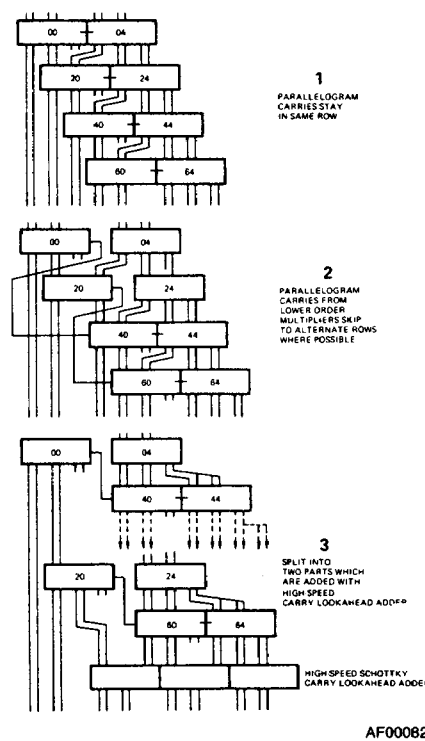

Figure 1

TYPICAL MULTIPLICATION TIMES

Array Size Bits	Total Multiplication Time (ns)	Package Count	
		Am25S05	Am54S/74S181
4 x 4	35	2	
8 x 8	75	8	
12 x 12	115	18	
12 x 12	82	18	5
16 x 16	155	32	
16 x 16	111	32	7
16 x 16	98	32	16
20 x 20	195	50	
20 x 20	130	50	9
24 x 24	235	72	
24 x 24	149	72	11
24 x 24	125	72	24
28 x 28	275	98	
28 x 28	168	98	13
32 x 32	315	128	
32 x 32	187	128	15
32 x 32	152	128	32

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$Y = (y_{-1}\ y_0\ y_1)\ 2^A$
$X = (x_{-1}\ x_0\ x_1\ x_2\ x_3)\ 2^B$

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Figure 2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Temperature(Ambient) Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 24 to Pin 12) Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.3		Volts
			XC	2.7	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., Y_1 = .0V			120	175	mA

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor (See loading rules).

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 280Ω)

Parameters	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	4 4	8 9	12 14	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$		6 5	12 10	18 15	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$		7 6	15 13	22 20	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}		3 5	6.5 10	12 15	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$		6 4	13.5 9.5	20 14	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$		3 3	15.5 12.5	23 19	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}		8 9	17 18	26 27	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$		10 10	21 21	32 32	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$		6 5	23.5 21.5	35 32	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}		11 10	23 20	34 30	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$		11 11	23 23	34 34	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$		12 12	25 25	37 37	ns

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Refer to Page 13-1 for Essential Information on Military Devices