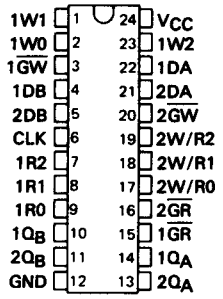
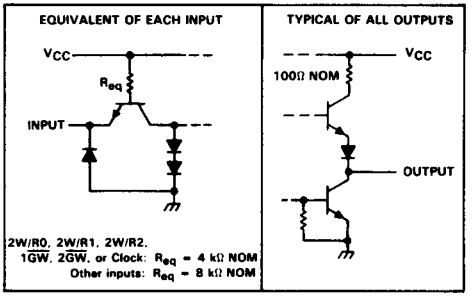
MAY 1972–REVISED MARCH 1988

- Independent Read/Write Addressing Permits Simultaneous Reading and Writing
- Organized as Eight Words of Two Bits Each
- Fast Access Times:
  From Read Enable . . . 15 ns Typical
  From Read Select . . . 33 ns Typical
- 3-State Outputs Simplify Use in Bus-Organized Systems
- Applications:
  Stacked Data Registers
  Scratch-Pad Memory
  Buffer Storage Between Processors
  Fast Multiplication Schemes

SN74172 . . . N PACKAGE
(TOP VIEW)



schematics of inputs and outputs



description

The SN74172, containing the equivalent of 201 gates on a monolithic chip, is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure 1).

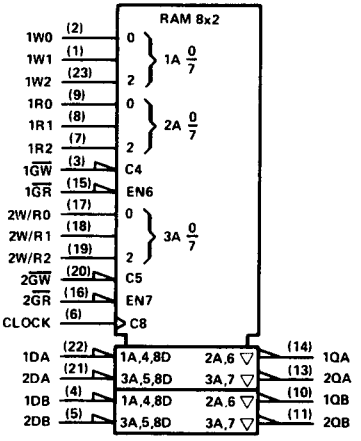
Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits
2) Reading from two bits
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

description (continued)

The three-state outputs of this register file permit connection of up to 129 compatible outputs and one Series 54/74 high-logic-level load to a common system bus. The outputs are controlled by the read-enable circuitry so that they operate as standard TTL totem-pole outputs when the appropriate read-enable input is low or they are placed in a high-impedance state when the associated read-enable input is at a high logic level. To minimize the possibility that two outputs from separate register files will attempt to take a common bus to opposite logic levels, the read-enable circuitry is designed such that disable times are shorter than enable times.

All inputs are buffered to lower the drive requirements of the clock, read/write address, and write-enable inputs to one normalized Series 54/74 load, and of all other inputs to one-half of one normalized Series 54/74 load.

Functions of the inputs and outputs of the SN74172 are as shown in the following table.

FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	$1\overline{GW}$	$2\overline{GW}$	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA ≠ 2DA and/or 1DB ≠ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	$1\overline{GR}$	$2\overline{GR}$	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

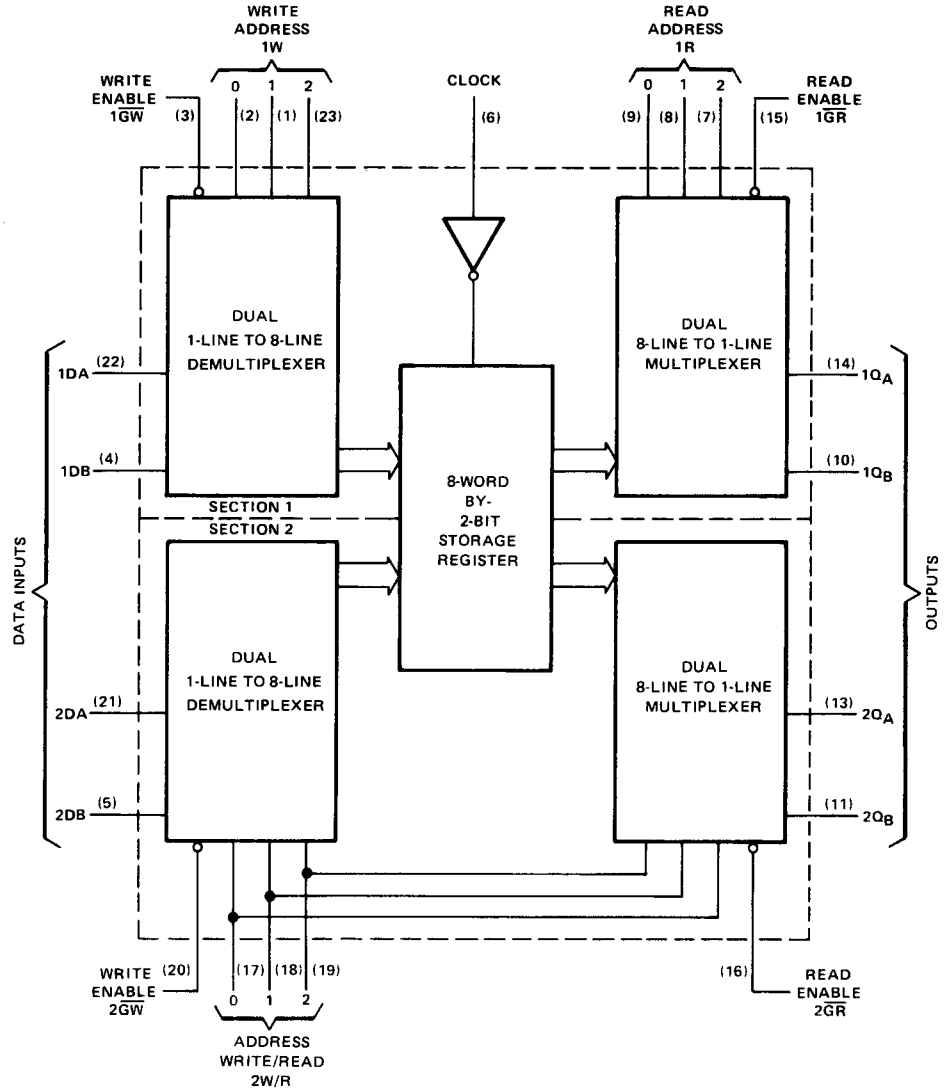

WRITE ADDRESS 1W
READ ADDRESS 1R
WRITE ENABLE 1GW
CLOCK
READ ENABLE 1GR
0 1 2
(3) (2) (1) (23)
(6)
(9) (8) (7) (15)
DUAL 1-LINE TO 8-LINE DEMULTIPLEXER
DUAL 8-LINE TO 1-LINE MULTIPLEXER
8-WORD BY-2-BIT STORAGE REGISTER
SECTION 1
SECTION 2
1DA (22)
1DB (4)
2DA (21)
2DB (5)
(14) 1QA
(10) 1QB
(13) 2QA
(11) 2QB
DATA INPUTS
OUTPUTS
WRITE ENABLE 2GW (20)
(17) (18) (19)
(16)
READ ENABLE 2GR
ADDRESS WRITE/READ 2W/R

FIGURE 1

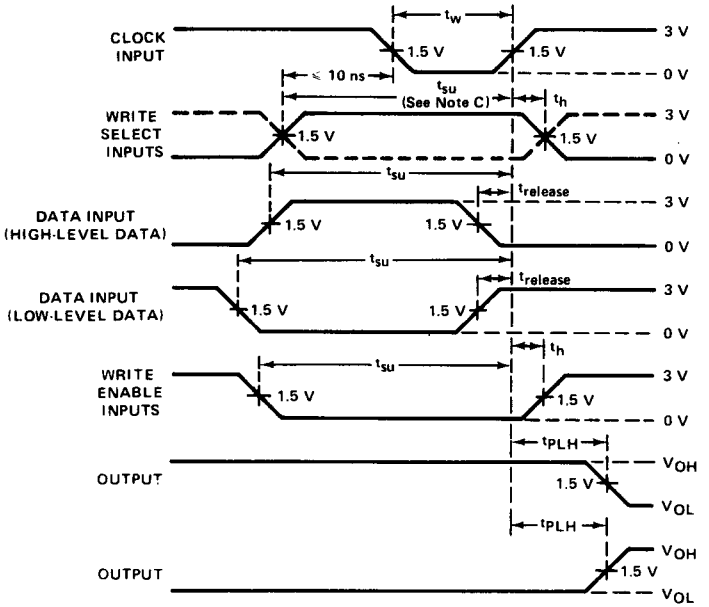
PC Board Considerations

Power Planes

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, See Figure 2	20			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from read select			33	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output from read select			30	45	
t_{PLH}	Propagation delay time, low-to-high-level output from clock			35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			35	50	
t_{PZH}	Output enable time to high level			14	30	ns
t_{PZL}	Output enable time to low level			16	30	
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Figure 2		6	20	ns
t_{PLZ}	Output disable time from low level			11	20	

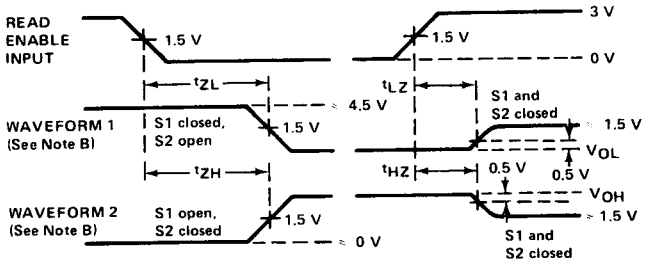
PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES FROM CLOCK INPUT

VOLTAGE WAVEFORMS
FIGURE 2

PARAMETER MEASUREMENT INFORMATION



ENABLE AND DISABLE TIMES FROM READ ENABLE

NOTES: A. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq$ ns, PRR ≈ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled. Waveform 2 is for an output with internal conditions such that the output is high except when disabled.
C. Write select setup time, as specified, will protect data written into previous address.
D. Load circuit is shown on page

VOLTAGE WAVEFORMS
FIGURE 2 (continued)

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