

# MITSUBISHI MICROCOMPUTERS M5L8042-XXXP

6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11654 D

SLAVE MICROCOMPUTER

T-49-19-05

## DESCRIPTION

The M5L8042-XXXP is a general-purpose programmable interface device designed for use with a variety of 8-bit microcomputer systems. The device is fabricated using n-channel silicon-gate ED-MOS technology.

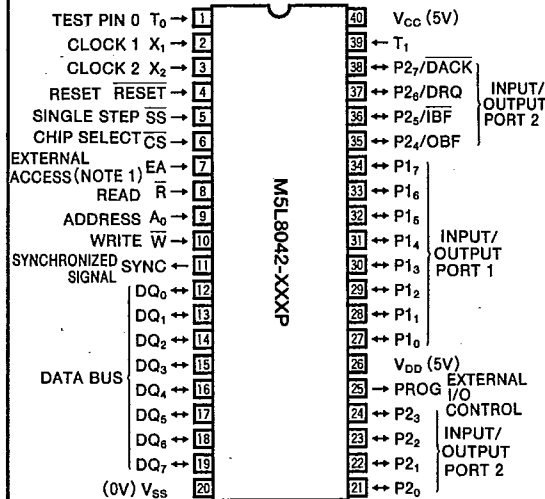
## FEATURES

- Mask ROM..... 2048-word by 8-bit
- Static RAM..... 128-word by 8-bit
- 18 programmable I/O pins
- Asynchronous data register for interface to master processor
- 8-bit CPU, ROM, RAM, I/O, timer, clock and low-power stand-by mode
- Single 5V power supply
- Alternative to custom LSI
- Interchangeable with i8042

## APPLICATION

Alternative to custom LSI for peripheral interfaces

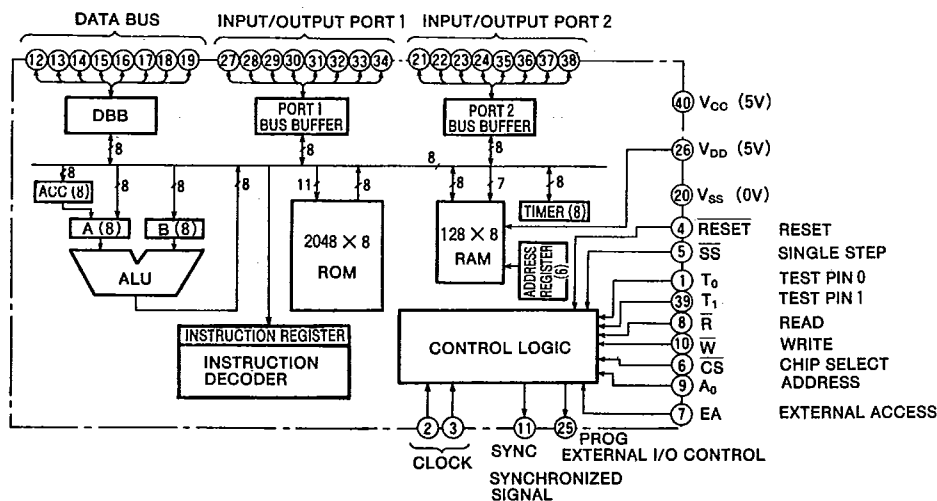
## PIN CONFIGURATION (TOP VIEW)



Outline 40P4

Note 1 : Connect to V<sub>SS</sub> in the operating condition.

## BLOCK DIAGRAM



**MITSUBISHI MICROCOMPUTERS**  
**M5L8042-XXXP**

6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11655 D  
**SLAVE MICROCOMPUTER**

T-49-19-05

**FUNCTION**

The M5L8042-XXXP is designed as an ordinary 8-bit CPU peripheral LSI chip and it contains a small stand-alone microcomputer. Although this microcomputer functions independently, when it is used as a peripheral controller, it is called the slave microcomputer in contrast to the master computer. These two devices can transfer the data alternatively through the buffer register between them. The

M5L8042-XXXP contains the buffer register to use this LSI as a slave microcomputer and it can be accessed in the same way as other standard peripheral devices. Since the M5L8042-XXXP is a complete microcomputer, it is easy to develop a user-oriented mask-programmed peripheral LSI only by changing the control software.

**PIN DESCRIPTION**

Pin	Name	Input or output	Function
V <sub>SS</sub>	Ground	—	Connected to a 0V supply (ground).
V <sub>CC</sub>	Main power supply	—	Connected to a 5V supply.
V <sub>DD</sub>	Power supply	—	Connected to a 5V supply. Used as a memory hold when V <sub>CC</sub> is cut off.
T <sub>0</sub>	Test pin 0	Input	Provides external control of conditional program jumps (JTO/JNTO instructions).
X <sub>1</sub> , X <sub>2</sub>	Crystal inputs	Input	An internal clock circuit is provided so that by connecting an RC circuit or crystal to these input pins, the clock frequency can be determined. X <sub>1</sub> and X <sub>2</sub> can also be used to input an external clock signal.
RESET	Reset	Input	CPU initialization input.
SS	Single step	Input	Used to halt the execution of a command by the CPU. When used in combination with the SYNC signal, the command execution of the CPU can be halted every instruction to enable single step operation.
CS	Chip select input	Input	Chip select input for data bus control.
EA	External access	Input	Normally maintained at 0V.
R	Read enable signal	Input	Serves as the read signal when the master CPU is accepting data on the data bus from the M5L8042-XXXP.
A <sub>0</sub>	Address input	Input	An address input used to indicate whether the signal on the data bus is data or a command.
W	Write enable signal	Input	Serves as the write signal when the master CPU is outputting data from the bus to the M5L8042-XXXP.
SYNC	Sync signal output	Output	Output 1 time for each machine cycle.
DQ <sub>0</sub> ~DQ <sub>7</sub>	Data bus	Input/output	Three-state, bidirectional data bus. Data bus is used to interface the M5L8042-XXXP to a master system data bus.
P2 <sub>0</sub> ~P2 <sub>7</sub>	Port 2	Input/output	Quasi-bidirectional port. When used as an input port, FF <sub>16</sub> must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary. P2 <sub>0</sub> ~P2 <sub>3</sub> are used when the M5L8243P I/O expander is used.
PROG	Program	Output	Serves as the strobe signal when the M5L8243P I/O expander is used.
P1 <sub>0</sub> ~P1 <sub>7</sub>	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF <sub>16</sub> must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary.
T <sub>1</sub>	Test pin 1	Input	Provides external control of conditional program jumps (JTI/JNTI instructions). Can serve as the input pin for the event counter (STRT CNT instruction).

**MITSUBISHI MICROCOMPUTERS**  
**M5L8042-XXXP**

6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11656 D

**SLAVE MICROCOMPUTER**

T-49-19-05

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Limits	Unit
V <sub>CC</sub>	Supply voltage	With respect to V <sub>SS</sub>	-0.5~7	V
V <sub>DD</sub>	Supply voltage		-0.5~7	V
V <sub>I</sub>	Input voltage		-0.5~7	V
V <sub>O</sub>	Output voltage		-0.5~7	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	1500	mW
T <sub>opr</sub>	Operating temperature range		0~70	°C
T <sub>stg</sub>	Storage temperature range		-65~150	°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>DD</sub>	Supply voltage	4.5	5	5.5	V
V <sub>SS</sub>	Supply voltage		0		V
V <sub>IH</sub>	High-level input voltage	2.2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
f <sub>(c)</sub>	Operating frequency	1		12	MHz

**ELECTRICAL CHARACTERISTICS** (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IL</sub>	Low-level input voltage		-0.5		0.8	V
V <sub>IH1</sub>	High-level input voltage (all except X <sub>1</sub> , X <sub>2</sub> , RESET)		2.2		V <sub>CC</sub>	V
V <sub>IH2</sub>	High-level input voltage (X <sub>1</sub> , X <sub>2</sub> , RESET)		3.8		V <sub>CC</sub>	V
V <sub>OL1</sub>	Low-level output voltage (DQ <sub>0</sub> ~DQ <sub>7</sub> )	I <sub>OL</sub> = 2mA			0.45	V
V <sub>OL2</sub>	Low-level output voltage (P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , SYNC)	I <sub>OL</sub> = 1.6 mA			0.45	V
V <sub>OL3</sub>	Low-level output voltage (PROG)	I <sub>OL</sub> = 1mA			0.45	V
V <sub>OH1</sub>	High-level output voltage (DQ <sub>0</sub> ~DQ <sub>7</sub> )	I <sub>OH</sub> = -400μA	2.4			V
V <sub>OH2</sub>	High-level output voltage (all other outputs)	I <sub>OH</sub> = -50μA	2.4			V
I <sub>I</sub>	Input leakage current (T <sub>0</sub> , T <sub>1</sub> , R, W, CS, A <sub>0</sub> , EA)	V <sub>SS</sub> ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10		10	μA
I <sub>OZL</sub>	High-impedance state output leakage current (DQ <sub>0</sub> ~DQ <sub>7</sub> )	V <sub>SS</sub> + 0.45 ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10		10	μA
I <sub>IL1</sub>	Low-level input load current (P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> )	V <sub>IL</sub> = 0.8V	-0.5			mA
I <sub>IL2</sub>	Low-level input load current (RESET, SS)	V <sub>IL</sub> = 0.8V	-0.2			mA
I <sub>DD</sub>	Supply current from V <sub>DD</sub>				10	mA
I <sub>CC</sub> + I <sub>DD</sub>	Total supply current				145	mA

MITSUBISHI MICROCOMPUTERS  
M5L8042-XXXP

6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11657 D

SLAVE MICROCOMPUTER

T-49-19-05

**TIMING REQUIREMENTS** ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ , unless otherwise noted)

**DBB Read**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_C (\#)$	Cycle time	$t_{CY}$		1.25		15	$\mu\text{s}$
$t_W (R)$	Read pulse width	$t_{RR}$	$t_C (\#) = 1.25 \mu\text{s}$	160			ns
$t_{SU} (CS-R)$	Chip select setup time before read	$t_{AR}$		0			ns
$t_H (R-CS)$	Chip select hold time after read	$t_{RA}$		0			ns

**DBB Write**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_W (W)$	Write pulse width	$t_{WW}$		160			ns
$t_{SU} (CS-W)$	$\overline{CS}$ , $A_0$ , setup time before write	$t_{AW}$		0			ns
$t_H (W-CS)$	$\overline{CS}$ , $A_0$ , hold time after write	$t_{WA}$		0			ns
$t_H (W-A0)$							ns
$t_{SU} (DQ-W)$	Data setup time before write	$t_{DW}$		130			ns
$t_H (W-DQ)$	Data hold time after write	$t_{WD}$		0			ns

**Port 2**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_W (PR)$	PROG pulse width	$t_{PP}$		700			ns
$t_{SU} (PC-PR)$	Port control setup time before PROG	$t_{CP}$	$C_L = 80\text{pF}$	80			ns
$t_H (PR-PC)$	Port control hold time after PROG	$t_{PC}$	$C_L = 20\text{pF}$	60			ns
$t_{SU} (Q-PR)$	Output data setup time before PROG	$t_{DP}$	$C_L = 80\text{pF}$	200			ns
$t_{SU} (D-PR)$	Input data hold time before PROG	$t_{PR}$	$C_L = 80\text{pF}$			650	ns
$t_H (PR-D)$	Input data hold time after PROG	$t_{PF}$	$C_L = 20\text{pF}$	0		150	ns

**DMA**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{SU} (DACK-R)$	DACK setup time before read	$t_{ACC}$		0			ns
$t_H (R-DACK)$	DACK hold time after read	$t_{CAC}$		0			ns
$t_{SU} (DACK-W)$	DACK setup time before write	$t_{ACC}$		0			ns
$t_H (W-DACK)$	DACK hold time after write	$t_{CAC}$		0			ns

Note 1 : Input voltage level  $V_{IL} = 0.45V$ ,  $V_{IH} = 2.4V$ .

**SWITCHING CHARACTERISTICS** ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ , unless otherwise noted)

**DBB Read**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX} (CS-DQ)$	Data enable time after $\overline{CS}$	$t_{AD}$	$C_L = 100\text{pF}$			130	ns
$t_{PZX} (A0-DQ)$	Data enable time after address	$t_{AD}$	$C_L = 100\text{pF}$			130	ns
$t_{PZX} (R-DQ)$	Data enable time after read	$t_{RD}$	$C_L = 100\text{pF}$			130	ns
$t_{PZX} (R-DQ)$	Data disable time after read	$t_{DF}$				85	ns

**DMA**

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX} (DACK-DQ)$	Data enable time after DACK	$t_{ACD}$	$C_L = 150\text{pF}$			130	ns
$t_{PHL} (R-DQ)$	DRQ disable time after read	$t_{CRO}$				90	ns
$t_{PHL} (W-DQ)$	DRQ disable time after write	$t_{CRO}$				90	ns

Note 2 : Output voltage discriminating levels, low and high, are 0.8V and 2.0V respectively.

MITSUBISHI MICROCOMPUTERS  
**M5L8042-XXXP**

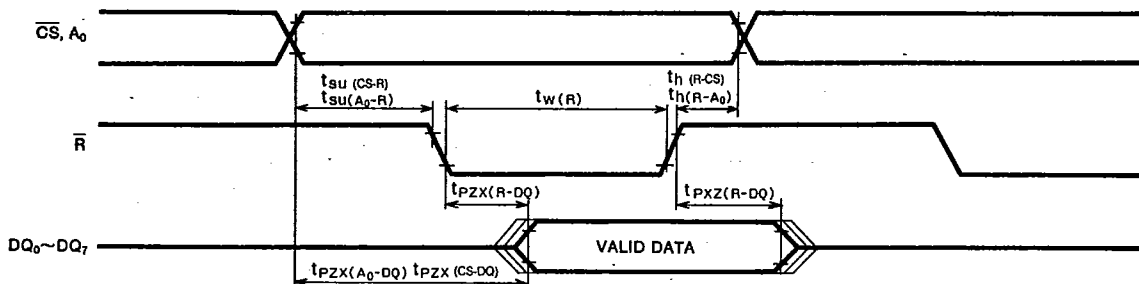
6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11658 D  
**SLAVE MICROCOMPUTER**

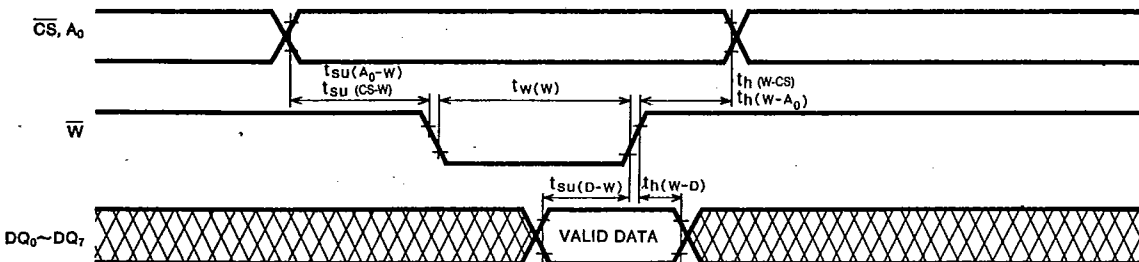
**TIMING DIAGRAMS**

T-49-19-05

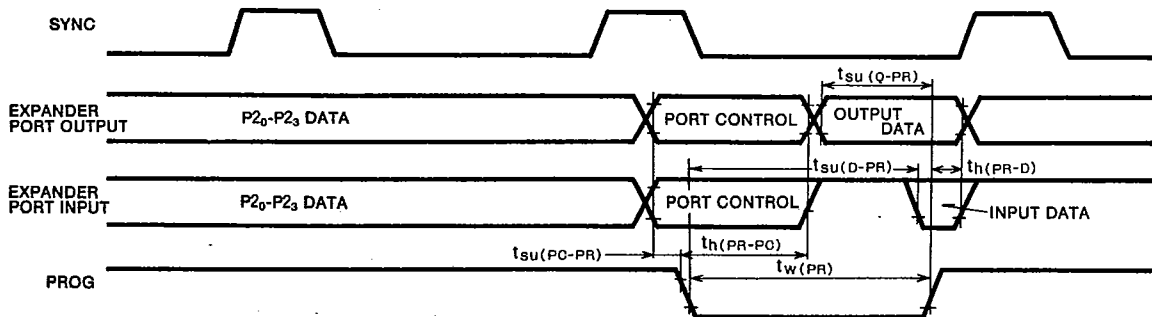
**Read**



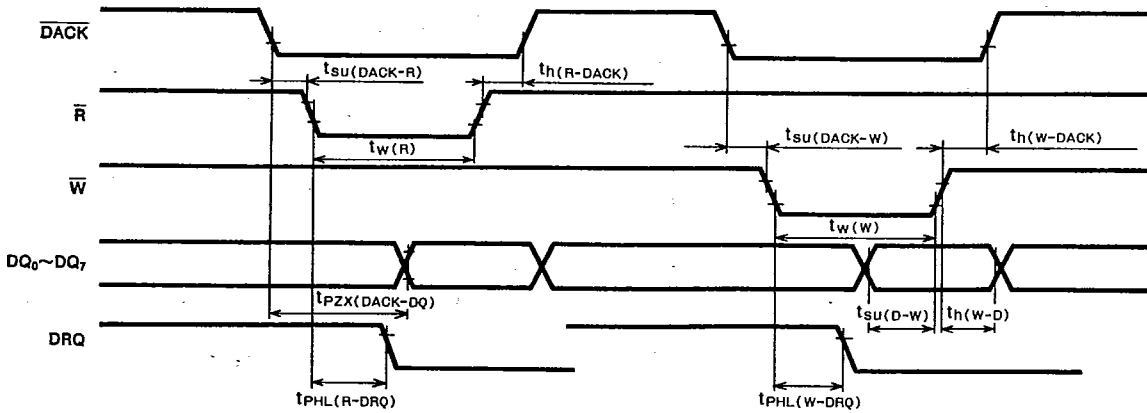
**Write**



**Port 2**



**DMA**



MITSUBISHI MICROCOMPUTERS

**M5L8042-XXXP**

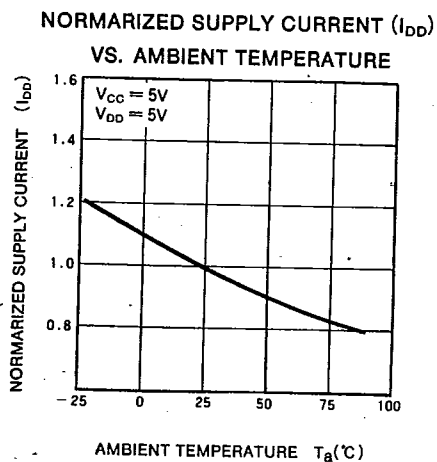
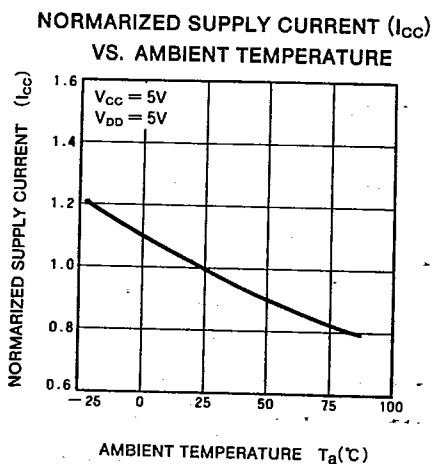
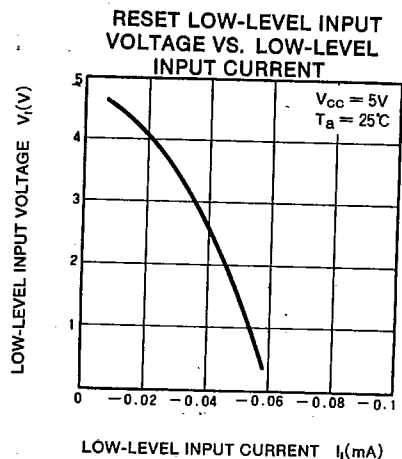
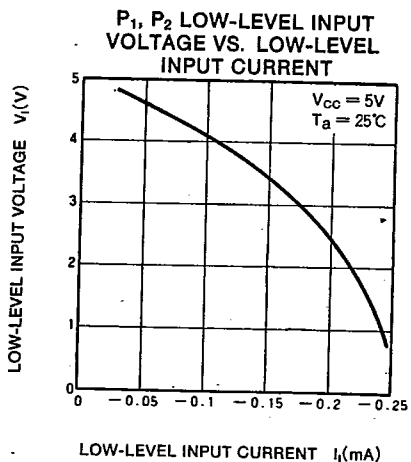
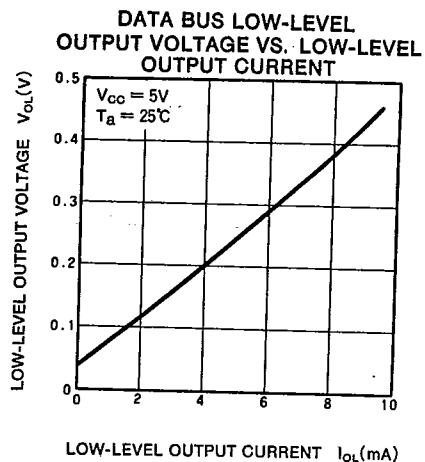
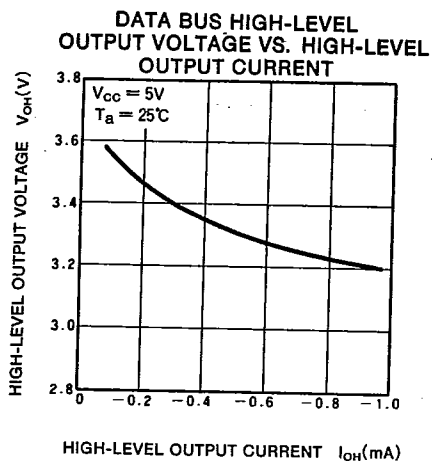
6249828 MITSUBISHI (MICMPTR/MIPRC)

91D 11659 D

SLAVE MICROCOMPUTER

T-49-19-05

TYPICAL CHARACTERISTICS



MITSUBISHI MICROCOMPUTERS  
**M5L8042-XXXP**

6249828 MITSUBISHI (MICMPTR/MIPRC)

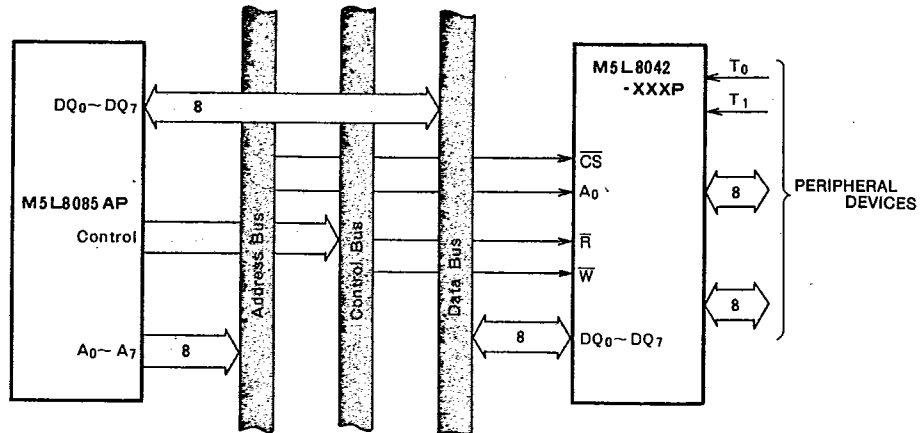
91D 11660 D

SLAVE MICROCOMPUTER

T-49-19-05

**APPLICATION EXAMPLES**

(1) Interface with M5L8085AP



(2) Interface with Series MELPS 8-48 Microcomputer and M5L8243P

